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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/760,431
Filing Date: January 20, 2004
Appellant(s): AVERILL ET AL.

Roy W. Truelson
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed June 4, 2007 appealing from the Office action mailed December 5, 2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,108,764	Baumgartner	8-2000
6,115,804	Carpenter	9-2000
2003/0009643	Arimilli	1-2003

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 5-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baumgartner (6,108,764) in view of Arimilli (2003/0009643).

As per claim 1, Baumgatner discloses a digital data processing system, comprising: a memory [Fig. 1; *memory 18*]; at least one processor having at least one associated cache for temporarily caching data from said memory [Fig. 1; *processor 12; cache 14*]; at least one device having a device cache, said device cache having a fixed number of slots for caching data, each slot caching a cache line of data [Fig. 1; *10a-10m*]; and a cache coherency mechanism, said cache coherency mechanism including a

cache line state directory structure, said cache coherency mechanism selectively determining whether to send cache line invalidation messages to said at least one device using state information in said cache line state directory structure, wherein at least a portion of said cache line state directory structure contains a plurality of cache line entries, each entry corresponding to a respective one of said plurality of slots for caching data of said device cache [Fig. 2; *Directory control logic 58; Coherency Response Logic 56; Transaction Send Unit (TSU); Data Send Unit (DSU); Transaction Receive Unit (TRU); Data Receive Unit (DRU)*; Table V, Table VI].

However, Baumgartner does explicitly teach a portion of the cache line state directory associated with the at least one device contains exactly a fixed number of cache line entries, each entry having a fixed correspondence to a unique one of the fixed number of slots as claimed.

Arimilli discloses a portion of the cache line state directory associated with at least one device containing exactly a fixed number of cache line entries, each entry having a fixed correspondence to a unique one of the fixed number of slots [par. 56] to provide a NUMA architecture having improved queing, storage and/or communication efficiency (par. 11).

Since the technology for implementing a computer system with a portion of the cache line state directory associated with at least one device containing exactly a fixed number of cache line entries, each entry having a fixed correspondence to a unique one of the fixed number of slots was well known as evidence by Arimilli, an artisan would have been motivated to implement this feature in the system of Baumgartner in order to

provide a NUMA architecture having improved queing, storage and/or communication efficiency. Thus, it would have been obvious to one of ordinary skill in the art, at the time of invention by Applicant to modify the system of Baumgartner to include a portion of the cache line state directory associated with at least one device containing exactly a fixed number of cache line entries, each entry having a fixed correspondence to a unique one of the fixed number of slots since this would have provided a NUMA architecture having improved queing, storage and/or communication efficiency (par. 11) as taught by Arimilli.

As per claim 2, Baumgatner discloses wherein said device is an I/O bridge device [Fig. 1; I/O devices 32 and Mezzanine bus 30].

As per claim 5, Baumgartner discloses said digital data processing system comprises a plurality of nodes, each node containing at least one processor, a respective portion of said memory, and a respective portion of said cache coherency mechanism [Fig. 3A].

As per claim 6, Baumgartner discloses each said respective portion of said cache coherency mechanism in each respective node maintains cache line state information for cached data having a real address in the respective portion of said memory contained in the node [Fig. 3B].

As per claim 7, Baumgartner discloses wherein each said respective portion of said cache coherency mechanism in each respective node maintains cache line state information for data cached in devices contained in the node [Fig. 3B].

As per claim 8, the rationale in the rejection of claim 1 is herein incorporated. Baumgartner further discloses wherein said digital data processing system comprises a plurality of devices having respective device caches, each said device cache having a respective fixed number of slots for caching data, each slot caching a cache line of data [Fig. 1]; and wherein said cache line state directory structure includes a plurality of portions, each portion corresponding to a respective one of said plurality of devices, each portion containing a plurality of cache line entries, each entry corresponding to a respective one of said plurality of slots for caching data of the device cache to which the respective portion corresponds [Fig. 2].

Claims 3-4, 9-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baumgartner (6,108,764) in view of Arimilli (2003/0009643), and further in view of Carpenter (6,115,804).

As per claim 3, Baumgatner discloses wherein a processor portion of said cache line state directory structure contains cache line state for at least one said cache associated with a processor, [col. 7, ll 59-67].

However, Baumgartner does not specifically teach said cache coherency mechanism further selectively determining whether to send cache line invalidation messages to the processor with which the cache is associated using state information in said processor portion of said cache line directory structure as required.

Carpenter discloses said cache coherency mechanism further selectively determining whether to send cache line invalidation messages to the processor with which the cache is associated using state information in said processor portion of said cache line directory structure [col. 12, ll 1-34] to concurrently store an unmodified copy of a particular cache line in a recent coherency state from which the copy of the particular cache line can be sourced by shared intervention (col. 3, ll 1-5).

Since the technology for implementing a computer system having multiple caches with sending cache line invalidation messages to the processor with which the cache is associated using state information in said processor portion of said cache line directory structure was well know as evidenced by Carpenter, an artisan would have been motivated to implement this feature in the system of Baumgartner in order to concurrently store an unmodified copy of a particular cache line in a recent coherency state from which the copy of the particular cache line can be sourced by shared intervention. Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by Applicant to modify the system of Baumgartner to include sending cache line invalidation messages to the processor with which the cache is associated using state information in said processor portion of said cache line directory structure because it was well known to concurrently store an unmodified copy of a particular

cache line in a recent coherency state from which the copy of the particular cache line can be sourced by shared intervention (col. 3, ll 1-5) as taught by Carpenter.

However, Baumgartner and Carpenter do not explicitly teach the processor portion being separate from the at least a portion of the cache line state directory structure associated with the at least one device, the processor portion containing a plurality of cache line entries, each entry having a fixed correspondence to a respective set of real addresses as claimed.

Arimilli discloses the processor portion being separate from the at least a portion of the cache line state directory structure associated with the at least one device, the processor portion containing a plurality of cache line entries, each entry having a fixed correspondence to a respective set of real addresses [Fig. 4; pars 0056, 0058] to provide a NUMA architecture having improved queing, storage and/or communication efficiency (par. 11).

Since the technology for implementing a computer system with the processor portion being separate from the at least a portion of the cache line state directory structure associated with the at least one device was well known as evidence by Arimilli, an artisan would have been motivated to implement this feature in the system of Baumgartner and Carpenter in order to provide a NUMA architecture having improved queing, storage and/or communication efficiency. Thus, it would have been obvious to one of ordinary skill in the art, at the time of invention by Applicant to modify the system of Baumgartner and Carpenter to include the processor portion being separate from the

at least a portion of the cache line state directory structure associated with the at least one device since this would have provided a NUMA architecture having improved queing, storage and/or communication efficiency (par. 11) as taught by Arimilli.

As per claim 4, Carpenter discloses wherein said processor portion of said cache line state directory structure contains cache line state for a plurality of caches associated with a plurality of processors, said cache coherency mechanism further selectively determining whether to send cache line invalidation messages to any of said plurality of processors using state information in said processor portion of said cache line directory structure [col. 11, ll 38-51].

As per claim 9, the rationale in the rejection of claims 3 and 8 is herein incorporated.

As per claim 10, the rationale in the rejection of claim 2 is herein incorporated.

As per claim 11, Carpenter discloses receiving a plurality of data access requests for cache lines of data from said device, each data access request from said device including data identifying a slot of said device cache in which the cache line will be stored [col. 11, ll 38-51]; and responsive to receiving each said data access request from said device, updating said cache line state directory structure by writing cache line identifying information corresponding to the data access request at the entry

corresponding to the slot in which the cache line requested by the data access request will be stored [col. 12, ll 1-34].

As per claim 12, Carpenter discloses wherein said step of maintaining a cache line state directory structure comprises maintaining a first portion of said cache line state directory structure corresponding to said device cache, and a second portion of said cache line state directory structure corresponding to a plurality of caches associated with a plurality of processors, said method further comprising the steps of: responsive to each of said plurality of data access requests, accessing said cache line state directory structure to determine whether data having a data address referenced by the request is contained in any of said plurality of processors [col. 11, ll 8-26]; for each of said plurality of data access requests, determining whether to send an invalidation message to any of said plurality of processors based on whether said step of accessing said cache line state directory structure determines that data having a data address referenced by the request is contained in any of said plurality of processors [col. 11, ll 38-51]; and for each of said plurality of data access requests, sending an invalidation message to at least one of said plurality of processors responsive to the determination made by said step of determining whether to send an invalidation message to any of said plurality of processors [col. 12, ll 1-34].

As per claim 13, the rationale in the rejection of claim 5 is herein incorporated.

As per claim 14, the rationale in the rejection of claim 9 is herein incorporated.

As per claim 15, the rationale in the rejection of claim 2 is herein incorporated.

As per claim 16, the rationale in the rejection of claim 5 is herein incorporated.

As per claim 17, Carpenter discloses wherein each said respective portion of said cache line state directory structure each respective node contains cache line state information for cached data having a real address in the respective portion of said memory contained in the node [Fig. 2].

As per claim 18, Carpenter discloses wherein each said respective portion of said cache line state directory structure each respective node contains cache line state information for data cached in devices contained in the node [Fig. 3A].

As per claim 19, the rationale in the rejection of claim 9 is herein incorporated. Baumgartner further discloses a cache coherency apparatus for a digital data processing system: a communications interface for communicating with a plurality of devices [Fig. 1]; and cache coherence control logic which selectively generates invalidation messages responsive to events affecting the validity of cached data, said cache coherence control logic determining whether to send cache line invalidation

messages to said first device using state information in said at least a portion of said cache line state directory structure corresponding to said cache in said first device [Fig. 2].

As per claim 20, the rationale in the rejection of claim 2 is herein incorporated.

As per claim 21, the rationale in the rejection of claim 3 is herein incorporated.

As per claim 22, Baumgartner discloses wherein said cache coherency apparatus is embodied in a single integrated circuit chip, said integrated circuit chip being separate from said first device [Fig. 2].

(10) Response to Argument

Appelant's arguments on page 9 of the remarks that "neither Baumgartner, Arimilli, nor Carpenter, alone or in combination, discloses the key features of appellant's independent claims, i.e., a cache line state directory used to send invalidation messages to a device, having a fixed a one-to-one correspondence with slots in the device cache" is clearly erroneous.

Examiner respectfully disagrees. Arimilli clearly discloses such limitation in at least paragraph [0056] where "cache 132 including a cache directory 140, data storage 130, and a cache controller 156. Data storage 130 is implemented as a set associative array organized as a number of congruence classes each containing a plurality of cache

lines. Cache directory 140, which records the contents of data storage 130 and associated state information includes a number of sets 142 that each correspond to a congruence class within data storage 130. Each set 142 contains a number of directory entries 144 for storing the address tag and coherency state of a corresponding cache line within the congruence class of data storage 130 with which the set 142 is associated (emphasis added)". Thus, it has been clearly shown that Arimilli teaches the feature of "a cache line state directory used to send invalidation messages to a device, having a fixed a one-to-one correspondence with slots in the device cache", verbatim in paragraph [0056]. As such, the claimed invention is not patentably distinct from the art of record.

Appellant's argument on page 10 of the remarks that "the cited art does not disclose or suggest a one-to-one correspondence" is respectfully traversed.

First of all Examiner would to point out that the limitation "a one-to-one correspondence" is nowhere recited in the claims and that such imitation has no basis in the claims and Applicants should not read limitations of the specification into the claims to thereby narrow the scope of the claims by implicitly adding disclosed limitations which have no express basis in the claims.

Arimilli discloses "request addresses including tag bits, index bits, and offset bits, where index bits of each request address received by cache 132 are input into cache directory 140, the index bits of the request address also select a set 142 within cache directory 140; a tag is stored within each entry 144 of the selected set 142. Thus,

Arimilli, clearly discloses "a separate portion of the cache line state directory contains entries for the processor cache or caches, and entries in the processor portion correspond to real addresses of data".

Baumgartner clearly discloses "coherency directory 50 storing indications of the system memory addresses (real addresses) of data (e.g., cache lines), the address indication for each cache line is stored in association with an identifier of each remote processing node having a copy of the cache line; col.7, ll 59-65". Thus, the association between the address indication for each cache line stored and an identifier of each remote processing node having a copy of that cache line, in Baumgartner, unequivocally defines a coherency directory with multiple entries with each entry having a one-to-one correspondence to a slot or entry in the cache.

Appellant's arguments on pages 12-13 of the remarks that "a cache directory structure as disclosed in Arimilli is not a cache coherency mechanism and that it is an entirely unrelated structure, which does not provide any sort of function similar to that recited in appellants' claims, i.e., that of determining whether to send an invalidation message to the associated cache" is clearly erroneous.

First of all, Examiner would like to point out that such argument has no bearing whatsoever on whether or not the cited teaches all the claimed limitations for a number of reasons: 1) Examiner never posits that the "cache directory" of Arimilli was equivalent to the "cache coherency mechanism" of the claimed invention. 2) Examiner never relied upon Arimilli in any of the Office Action for the teaching of a "cache coherence

mechanism". Baumgartner, rather, teaches such claimed feature as evident in all of the Office Actions.

Additionally, It is worth mentioning that Appellant's *cache coherency mechanism includes a cache line state directory structure and selectively determines whether to send cache line invalidation messages using state information...* and Arimilli likewise discloses "when a store request is received at a node, the node must broadcast a Flush (i.e., invalidate) operation to all other nodes indicated in the home node's local memory directory as holding the target cache line, for example, directory RMD 74 preferably stores not only address information related to data in RMC 70,but also coherency information, and coherency state of a corresponding cache line, as evidenced in pars. [0009, 0044, 0056]. As such, Arimilli similarly discloses the cache coherency mechanism of Appellant's claimed invention.

Appellant's argument that "the motivation for his invention is to avoid a situation in which a cache in an I/O bridge or similar device, having a small size and very large turnover, crowds out the other entries in the coherence directory structure and that this motivation is neither disclosed nor suggested by any of the cited references and finally concludes that the Examiner is relying on hindsight gleaned from Applellant's disclosure" is clearly erroneous.

Appellant's arguments in that respect are flawed for a number of reasons: 1) Appellant asserts that there could only be one motivation for "constructing a coherency directory having a one-to-one correspondence with one of the device caches"; 2)

Appellant presumes without justification that his motivation, i.e., "to avoid a situation in which a cache in an I/O bridge or similar device, having a small size and very large turnover, crowds out the other entries in the coherence directory structure", must be the motivation of everyone else; 3) Appellant assumes without any factual basis or evidence that his motivation must be the only motivation "for constructing a coherency directory having a one-to-one correspondence"; and 4) In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

Appellant's arguments on page 15 that "the division of the cache coherence structure into multiple parts having different organization is not disclosed or suggested by any of the cited art" is clearly erroneous.

First of all, dependent claim 12, does not recite "division of the cache coherence structure into multiple parts having different organization". Second of all, in response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., the division of the

cache coherence structure into multiple parts having different organization) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Finally, Arimilly discloses "associated state information, including a number of sets that each correspond to a congruence class; each set contains a number of directory entries for storing the address tag and coherency state of a corresponding cache line within the congruence class with which the set is associated; par. 0056".

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Mardochee Chery
Examiner

Conferees:

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